# LAB No 1

**INTRODUCTION TO MODELSIM AND GATE LEVEL MODELING**

**Objectives:**

Introduction to MODELSIM

# Software used:

MODELSIM

# MODELSIM:

MODELSIM is a simulator which can be used for the simulations of both VHDL and Verilog HDL. It has the following interface.

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# How to use MODELSIM?

**Step 1**

**Creating a new project**

Select **File > New > Project** (Main window) to create a new project. This opens the **Create Project** dialog.

The dialog includes these options:

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* + **Project Name**

The name of the new project.

* + **Project Location**

The directory in which the *.mpf* file will be created.

* + **Default Library Name**

The name of the working library.

You can generally leave the **Default Library Name** set to "work." The name you specify will be used to create a working library subdirectory within the Project Location.

After selecting OK, you will see a blank Project tab in the workspace area of the Main window and the

**Add Items to the Project** dialog.

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The name of the current project is shown at the bottom left corner of the Main window.

**Step 2**

**Adding items to the project**

The **Add Items to the Project** dialog includes these options:

**Create New File**

Create a new VHDL, Verilog, Tcl, or text file using the Source window. See below for details.

**Add Existing File**

Add an existing file. See below for details.

**Create Simulation**

Create a Simulation Configuration that specifies source files and simulator options. See

**Create New Folder**

Create an organization folder.

***Create New File***

The **Create New File** command lets you create a new VHDL, Verilog, Tcl, or text file using the Source window. You can also access this command by selecting **File > Add to Project > New File** (Main window) or right- clicking (2nd button in Windows; 3rd button in UNIX) in the Project tab and selecting **Add to Project > New File**.

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The **Create Project File** dialog includes these options:

**File Name**

**Add file as type Folder**

The name of the new file

Add the type of the new file. Select VHDL, Verilog, TCL, or text.

The organization folder in which you want the new file placed. You must first create folders in order to access them here

When you select OK, the Source window opens with an empty file, and the file is listed in the Project tab of the Main window workspace.

***Add Existing File***

You can also access this command by selecting **File > Add to Project > Existing File** (Main window) or by right-clicking (2nd button in Windows; 3rd button in UNIX) in the Project tab and selecting **Add to Project > Existing File**.

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The **Add file to Project** dialog includes these options:

**File Name**

The name of the file to add. You can add multiple files at one time.

**Add file as type**

The type of the file. "Default" assigns type based on the file extension (e.g., *.v* is type Verilog).

**Folder**

The organization folder in which you want the file placed. You must first create folders in order to access them here. Choose whether to reference the file from its current location or to copy it into the project directory. When you select OK, the file(s) is listed in the Project tab of the Main window workspace.

**Step 3**

**Compiling the files**

The question marks next to the files in the Project tab denote either the files haven’t been compiled into the project or the source has changed since the last compile. To compile the files, select **Compile > Compile All** (Main window) or right click in the Project tab and select **Compile > Compile All**.

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Once compilation is finished, click the Library tab, expand library *work* by clicking the "+", and you’ll see the two compiled design units.

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**Step 4**

**Simulating a design**

To simulate one of the designs, either double-click the name or right-click the name and select Simulate. A new tab appears showing the structure of the active simulation. At this point you are ready to run the simulation and analyze your results. You often do this by adding signals to the Wave window and running the simulation for a given period of time.

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# Program:

Example for the module instantiation

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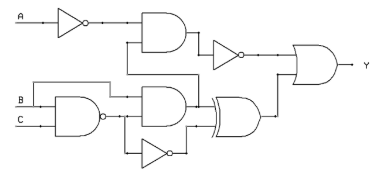
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# Lab tasks:

1. Implement a buffer at the gate level.
2. Implement an inverter at the gate level.
3. Implement an OR gate using a NAND gates.
4. Implement the following equation where z is output and x1, x2, x3, x4, and x5 are inputs of the circuit.

z = ( y1 + y2 )’ y1 = x1.x2

y2 = (x3.x4.x5)



Implement the above circuit where A,B and C are input to the circuit and Y is the output of the circuit .